74LV4066

Quad bilateral switches

Rev. 03 — 4 July 2005 **Product data sheet**

1. General description

The 74LV4066 is a low-voltage Si-gate CMOS device that is pin and function compatible with the 74HC4066 and 74HCT4066.

The 74LV4066 has four independent switches. Each switch has two input/output pins (nY, nZ) and an active HIGH enable input pin (nE). When nE is LOW the corresponding analog switch is turned off.

The 74LV4066 has a ON-resistance which is reduced in comparison with the 74HCT4066.

2. Features

- Optimized for low-voltage applications: 1.0 V to 3.6 V
- Typical V_{OLP} (output ground bounce): < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Very low ON-resistance:
  - 60 Ω (typical) at V_{CC} = 2.0 V
  - 35 Ω (typical) at V_{CC} = 3.0 V
  - 25 Ω (typical) at V_{CC} = 4.5 V
- ESD protection:
  - HBM EIA/JESD22-A114C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C

PHILIPS

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns; C_L = 15 pF; R_L = 1 kΩ.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PZL}, t_{PZH}	turn-on time nE to V_{os}	V_{CC} = 3.3 V		-	10	-	ns
t_{PLZ}, t_{PHZ}	turn-off time nE to V_{os}	V_{CC} = 3.3 V		-	13	-	ns
C_i	input capacitance			-	3.5	-	pF
C_S	maximum switch capacitance			-	8	-	pF
C_{PD}	power dissipation capacitance per switch	V_{CC} = 3.3 V	[1] [2]	-	11	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

C_S = maximum switch capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4066N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV4066D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV4066DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV4066PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

5. Functional diagram

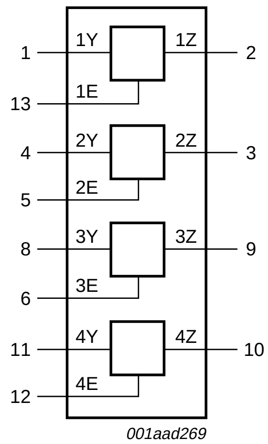


Fig 1. Logic symbol

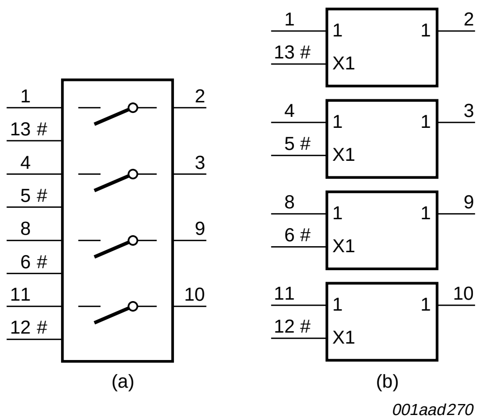


Fig 2. IEC logic diagram

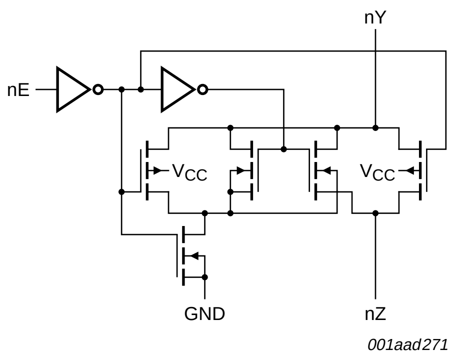


Fig 3. Logic diagram (one switch)

6. Pinning information

6.1 Pinning

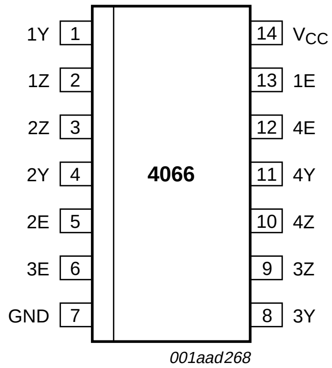


Fig 4. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1Y	1	independent input or output
1Z	2	independent output or input
2Z	3	independent output or input
2Y	4	independent input or output
2E	5	enable input
3E	6	enable input
GND	7	ground (0 V)
3Y	8	independent input or output
3Z	9	independent output or input
4Z	10	independent output or input
4Y	11	independent input or output
4E	12	enable input
1E	13	enable input
V_{CC}	14	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table

Input nE	Switch
LOW	off
HIGH	on

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±50	mA
I_S	switch source or sink current	$V_O = -0.5$ V to (V_{CC} + 0.5 V)	[1]	-	±25	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
	DIP14 package		[2]	-	750	mW
	SO14 package		[3]	-	500	mW
	(T)SSOP14 package		[4]		400	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] (T)SSOP14 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	6	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air		–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.0 V to 2.0 V		-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V		-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V		-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.90	-	-	V
		V_{CC} = 2.0 V	1.40	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.00	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.20	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.30	V
		V_{CC} = 2.0 V	-	-	0.60	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.80	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.80	V
I_{LI}	input leakage current	V_I = V_{CC} or GND				
		V_{CC} = 3.6 V	-	-	1.0	µA
		V_{CC} = 6.0 V	-	-	2.0	µA
$I_{S(OFF)}$	analog switch OFF-state current	V_I = V_{IH} or V_{IL}; see Figure 5				
		V_{CC} = 3.6 V	-	-	1.0	µA
		V_{CC} = 6.0 V	-	-	2.0	µA
$I_{S(ON)}$	analog switch ON-state current	V_I = V_{IH} or V_{IL}; see Figure 6				
		V_{CC} = 3.6 V	-	-	1.0	µA
		V_{CC} = 6.0 V	-	-	2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A				
		V_{CC} = 3.6 V	-	-	20	µA
		V_{CC} = 6.0 V	-	-	40	µA
ΔI_{CC}	additional supply current per input	V_I = V_{CC} – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.90	-	-	V
		V_{CC} = 2.0 V	1.40	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.00	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.20			V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.30	V
		V_{CC} = 2.0 V	-	-	0.60	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.80	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.80	V

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND				
		$V_{CC} = 3.6$ V	-	-	1.0	µA
		$V_{CC} = 6.0$ V	-	-	2.0	µA
$I_{S(OFF)}$	analog switch OFF-state current	$V_I = V_{IH}$ or V_{IL}; see Figure 5				
		$V_{CC} = 3.6$ V	-	-	1.0	µA
		$V_{CC} = 6.0$ V	-	-	2.0	µA
$I_{S(ON)}$	analog switch ON-state current	$V_I = V_{IH}$ or V_{IL}; see Figure 6				
		$V_{CC} = 3.6$ V	-	-	1.0	µA
		$V_{CC} = 6.0$ V	-	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A				
		$V_{CC} = 3.6$ V	-	-	40	µA
		$V_{CC} = 6.0$ V	-	-	80	µA
ΔI_{CC}	additional supply current per input	$V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.7$ V to 3.6 V	-	-	850	µA

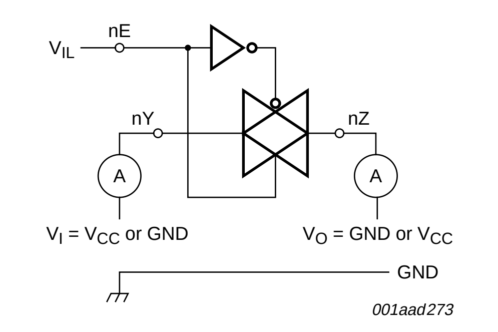


Fig 5. Test circuit for measuring OFF-state current

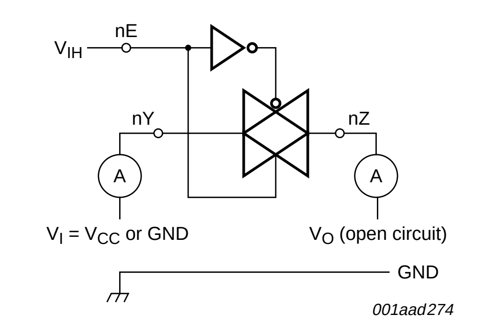


Fig 6. Test circuit for measuring ON-state current

Table 8: ON-resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]; see Figure 8							
$R_{ON(peak)}$	ON-resistance (peak)	$V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 1.2 V	[2]	-	300	-	Ω
		V_{CC} = 2.0 V		-	60	130	Ω
		V_{CC} = 2.7 V		-	41	60	Ω
		V_{CC} = 3.0 V to 3.6 V		-	37	72	Ω
		V_{CC} = 4.5 V		-	25	52	Ω
		V_{CC} = 6.0 V		-	23	47	Ω
$R_{ON(rail)}$	ON-resistance (rail)	$V_I = V_{IH}$ or V_{IL}; V_{is} = GND					
		V_{CC} = 1.2 V	[2]	-	75	-	Ω
		V_{CC} = 2.0 V		-	35	98	Ω
		V_{CC} = 2.7 V		-	26	60	Ω
		V_{CC} = 3.0 V to 3.6 V		-	24	52	Ω
		V_{CC} = 4.5 V		-	15	40	Ω
		V_{CC} = 6.0 V		-	13	35	Ω
		$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$					
		V_{CC} = 1.2 V	[2]	-	75	-	Ω
		V_{CC} = 2.0 V		-	40	110	Ω
		V_{CC} = 2.7 V		-	35	72	Ω
		V_{CC} = 3.0 V to 3.6 V		-	30	65	Ω
		V_{CC} = 4.5 V		-	22	47	Ω
		V_{CC} = 6.0 V		-	20	40	Ω
$R_{ON(flatness)}$	ON-resistance (flatness)	$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$					
		V_{CC} = 2.0 V		-	5	-	Ω
		V_{CC} = 2.7 V		-	4	-	Ω
		V_{CC} = 3.0 V to 3.6 V		-	4	-	Ω
		V_{CC} = 4.5 V		-	3	-	Ω
		V_{CC} = 6.0 V		-	2	-	Ω
T_{amb} = –40 °C to +125 °C							
$R_{ON(peak)}$	ON-resistance (peak)	$V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 2.0 V		-	-	150	Ω
		V_{CC} = 2.7 V		-	-	90	Ω
		V_{CC} = 3.0 V to 3.6 V		-	-	83	Ω
		V_{CC} = 4.5 V		-	-	60	Ω
		V_{CC} = 6.0 V		-	-	54	Ω

Table 8: ON-resistance *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{ON(rail)}$	ON-resistance (rail)	$V_I = V_{IH}$ or V_{IL}; V_{is} = GND				
		V_{CC} = 2.0 V	-	-	115	Ω
		V_{CC} = 2.7 V	-	-	68	Ω
		V_{CC} = 3.0 V to 3.6 V	-	-	60	Ω
		V_{CC} = 4.5 V	-	-	45	Ω
		V_{CC} = 6.0 V	-	-	40	Ω
		$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$				
		V_{CC} = 2.0 V	-	-	130	Ω
		V_{CC} = 2.7 V	-	-	85	Ω
		V_{CC} = 3.0 V to 3.6 V	-	-	75	Ω
		V_{CC} = 4.5 V	-	-	55	Ω
		V_{CC} = 6.0 V	-	-	47	Ω

[1] All typical values are measured at T_{amb} = 25 °C.

[2] At supply voltage approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

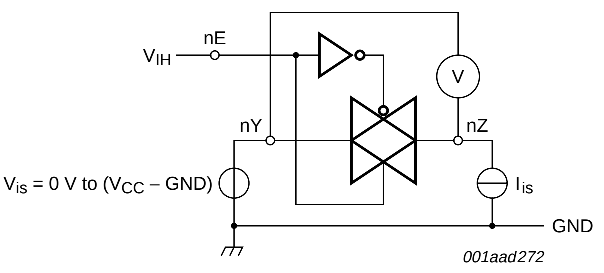


Fig 7. Test circuit for measuring ON-resistance

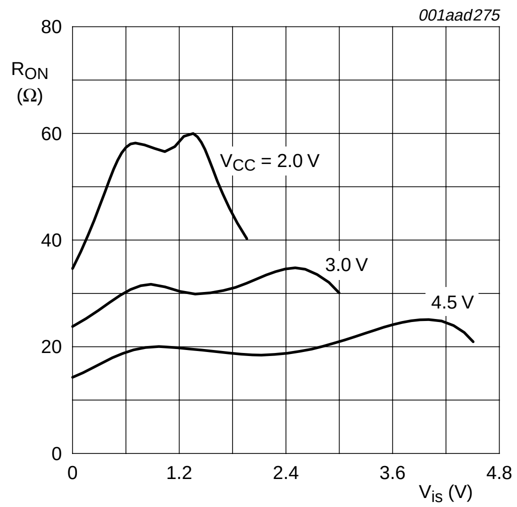


Fig 8. ON-resistance as a function of input voltage

11. Dynamic characteristics

Table 9: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	see Figure 9					
		V_{CC} = 1.2 V		-	8	-	ns
		V_{CC} = 2.0 V		-	5	26	ns
		V_{CC} = 2.7 V to 3.6 V		-	3	15	ns
		V_{CC} = 4.5 V		-	2	13	ns
		V_{CC} = 6.0 V		-	2	10	ns
t_{PZH}, t_{PZL}	turn-on time nE to V_{os}	see Figure 9					
		V_{CC} = 1.2 V		-	40	-	ns
		V_{CC} = 2.0 V		-	22	43	ns
		V_{CC} = 2.7 V to 3.6 V		-	12	25	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	10	-	ns
		V_{CC} = 4.5 V		-	10	21	ns
		V_{CC} = 6.0 V		-	8	16	ns
t_{PHZ}, t_{PLZ}	turn-off time nE to V_{os}	see Figure 9					
		V_{CC} = 1.2 V		-	50	-	ns
		V_{CC} = 2.0 V		-	27	65	ns
		V_{CC} = 2.7 V to 3.6 V		-	15	38	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	13	-	ns
		V_{CC} = 4.5 V		-	13	32	ns
		V_{CC} = 6.0 V		-	12	28	ns
C_{PD}	power dissipation capacitance per switch	V_{CC} = 3.3 V; C_L = 15 pF	[2] [3]	-	11	-	pF
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	see Figure 9					
		V_{CC} = 2.0 V		-	-	31	ns
		V_{CC} = 2.7 V to 3.6 V		-	-	18	ns
		V_{CC} = 4.5 V		-	-	15	ns
		V_{CC} = 6.0 V		-	-	12	ns
t_{PZH}, t_{PZL}	turn-on time nE to V_{os}	see Figure 9					
		V_{CC} = 2.0 V		-	-	51	ns
		V_{CC} = 2.7 V to 3.6 V		-	-	30	ns
		V_{CC} = 4.5 V		-	-	26	ns
		V_{CC} = 6.0 V		-	-	20	ns

Table 9: Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	turn-off time nE to V_{os}	see Figure 9				
		V_{CC} = 2.0 V	-	-	81	ns
		V_{CC} = 2.7 V to 3.6 V	-	-	47	ns
		V_{CC} = 4.5 V	-	-	40	ns
		V_{CC} = 6.0 V	-	-	34	ns

[1] Typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

C_S = maximum switch capacitance in pF;

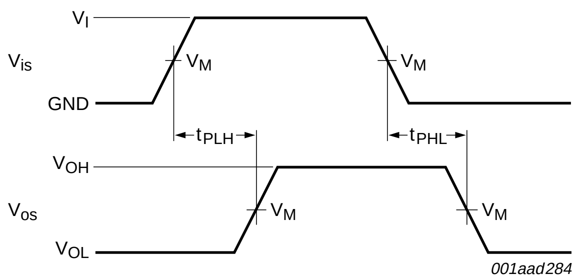
V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ = sum of the outputs.

[3] The condition is V_I = GND to V_{CC}.

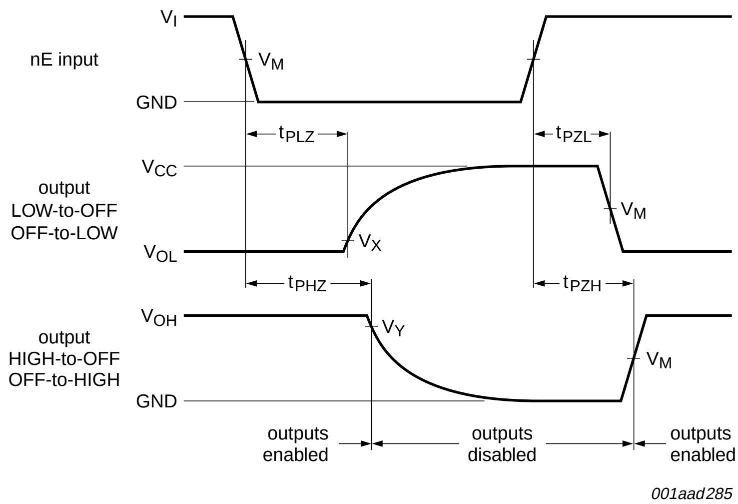
12. Waveforms



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 9. Input to output propagation delays



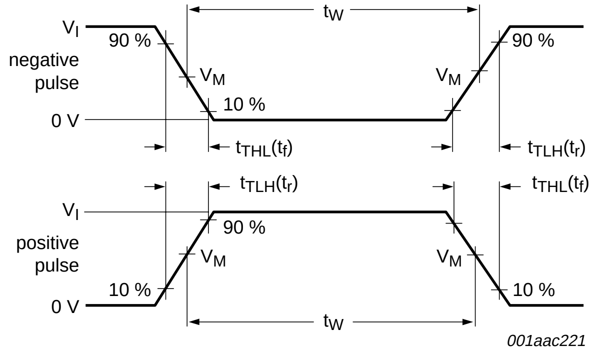
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

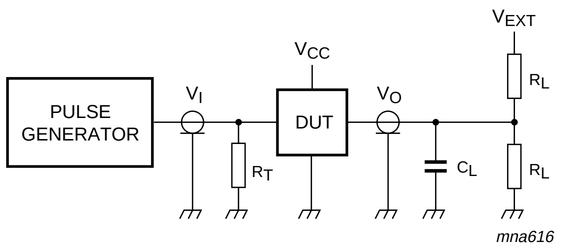
Fig 10. Turn-on and turn-off times for the inputs to the output

Table 10: Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
≥ 2.7 V	1.5 V	1.5 V	V_{OL} + 0.3	V_{OH} − 0.3 V
< 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15	V_{OH} − 0.15 V



a. Input pulse definition



Test data is given in Table 11.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 11. Load circuitry for switching times

Table 11: Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L [1]	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	GND	2 × V_{CC}	open
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	GND	2 × V_{CC}	open
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	GND	2 × V_{CC}	open

[1] $R_L = \infty$ Ω for measuring the propagation delays t_{PLH} and t_{PHL}.

13. Additional dynamic characteristics

Table 12: Additional dynamic characteristics

Voltages are referenced to GND (ground = 0 V); V_{is} is the input voltage at pin nY or nZ, whichever is assigned as an input; V_{os} is the output voltage at pin nY or nZ, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
d_{sin}	sine-wave distortion	R_L = 10 kΩ; f = 1 kHz; C_L = 50 pF; see Figure 12					
		V_{CC} = 3.0 V; V_{is} = 2.75 V (p-p)		-	0.04	-	%
		V_{CC} = 6.0 V; V_{is} = 5.50 V (p-p)		-	0.02	-	%
		R_L = 10 kΩ; f = 10 kHz; C_L = 50 pF; see Figure 12					
		V_{CC} = 3.0 V; V_{is} = 2.75 V (p-p)		-	0.12	-	%
		V_{CC} = 6.0 V; V_{is} = 5.50 V (p-p)		-	0.06	-	%
$\alpha_{OFF(feedthru)}$	switch OFF-state signal feed-through attenuation	R_L = 600 kΩ; f = 1 MHz; C_L = 50 pF; see Figure 13 and Figure 14	[1]				
		V_{CC} = 3.0 V		-	–50	-	dB
		V_{CC} = 6.0 V		-	–50	-	dB
$\alpha_{ct(S)}$	crosstalk between switches	R_L = 600 kΩ; f = 1 MHz; C_L = 50 pF; see Figure 15	[1]				
		V_{CC} = 3.0 V		-	–60	-	dB
		V_{CC} = 6.0 V		-	–60	-	dB
$V_{ct(pp)}$	crosstalk voltage between enable input to any switch (peak-to-peak value)	R_L = 600 kΩ; f = 1 MHz; C_L = 50 pF; see Figure 16 and Figure 17	[2]				
		V_{CC} = 3.0 V		-	110	-	mV
		V_{CC} = 6.0 V		-	220	-	mV
f_{max}	minimum frequency response (–3 dB)	R_L = 50 kΩ; C_L = 50 pF; see Figure 18 and Figure 19	[3]				
		V_{CC} = 3.0 V		-	180	-	MHz
		V_{CC} = 6.0 V		-	200	-	MHz
C_S	maximum switch capacitance			-	8	-	pF

[1] Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).

[2] Pin nE: square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns.

[3] Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

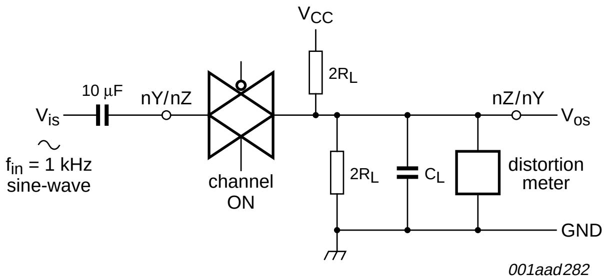


Fig 12. Test circuit for measuring sine-wave distortion

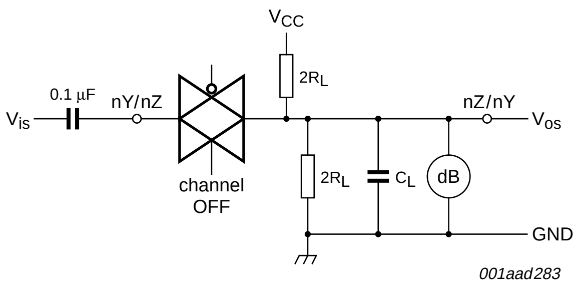
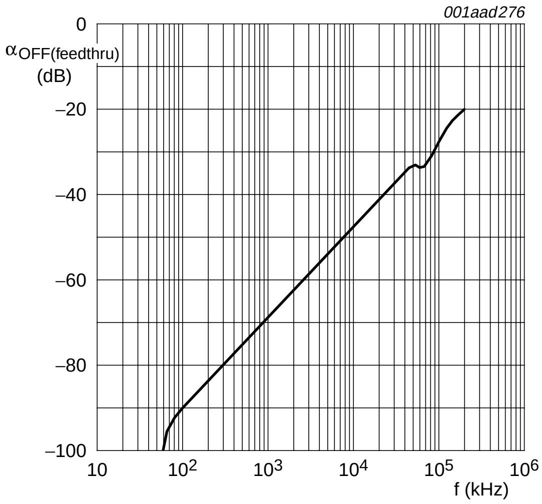
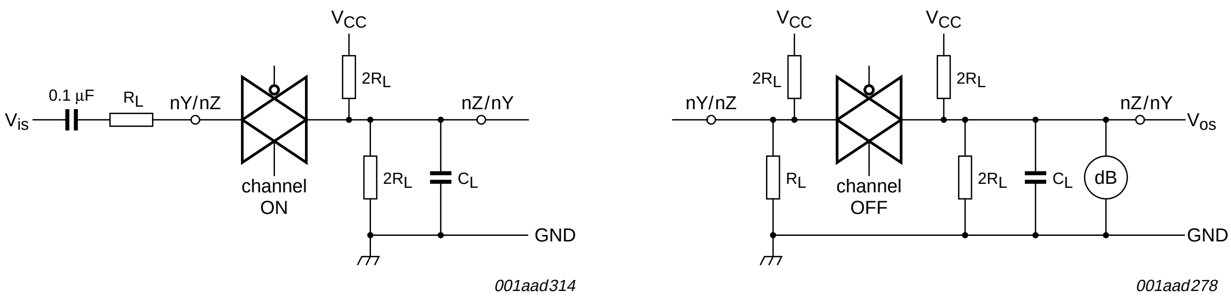


Fig 13. Test circuit for measuring switch OFF-state signal feed-through



V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω;
R_{SOURCE} = 1 kΩ.

Fig 14. Switch OFF-state signal feed-through as a function of frequency



a. Channel on condition

b. Channel off condition

Fig 15. Test circuit for measuring crosstalk between switches

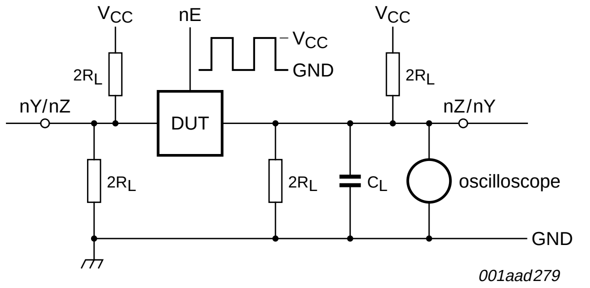


Fig 16. Test circuit for measuring crosstalk between enable and any switch

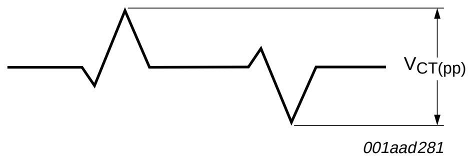


Fig 17. Crosstalk definition (oscilloscope output)

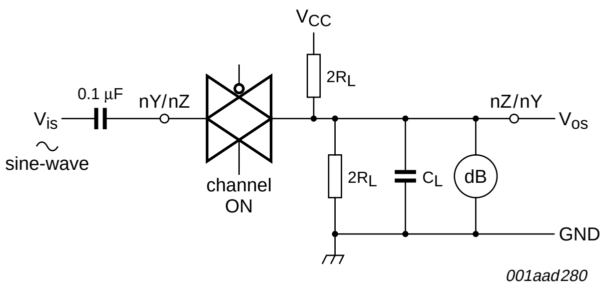
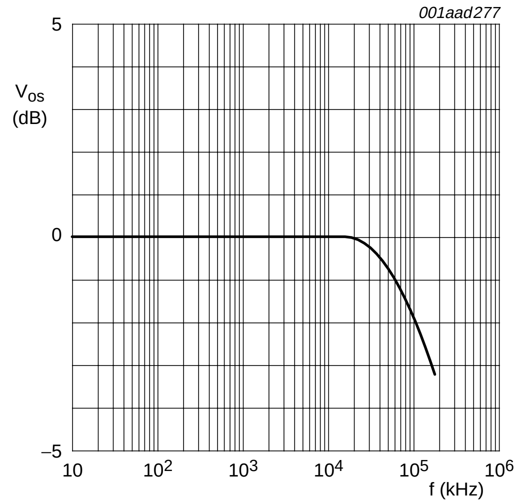


Fig 18. Test circuit for measuring minimum frequency response

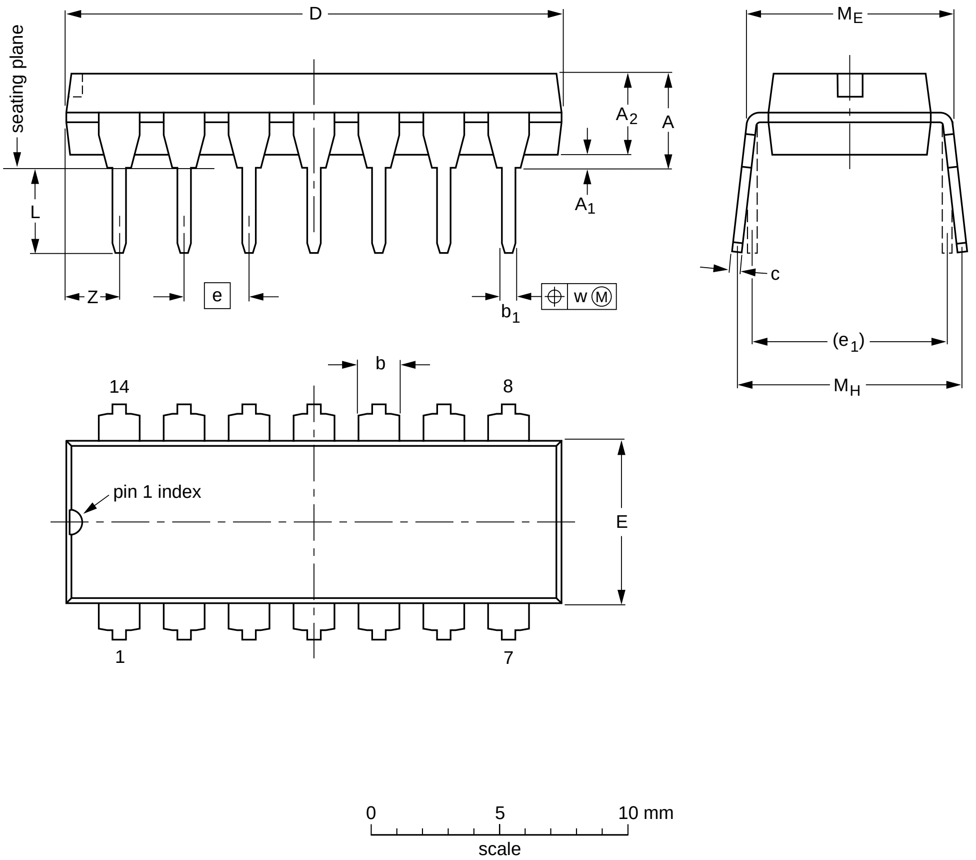


V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

Fig 19. Frequency response

14. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

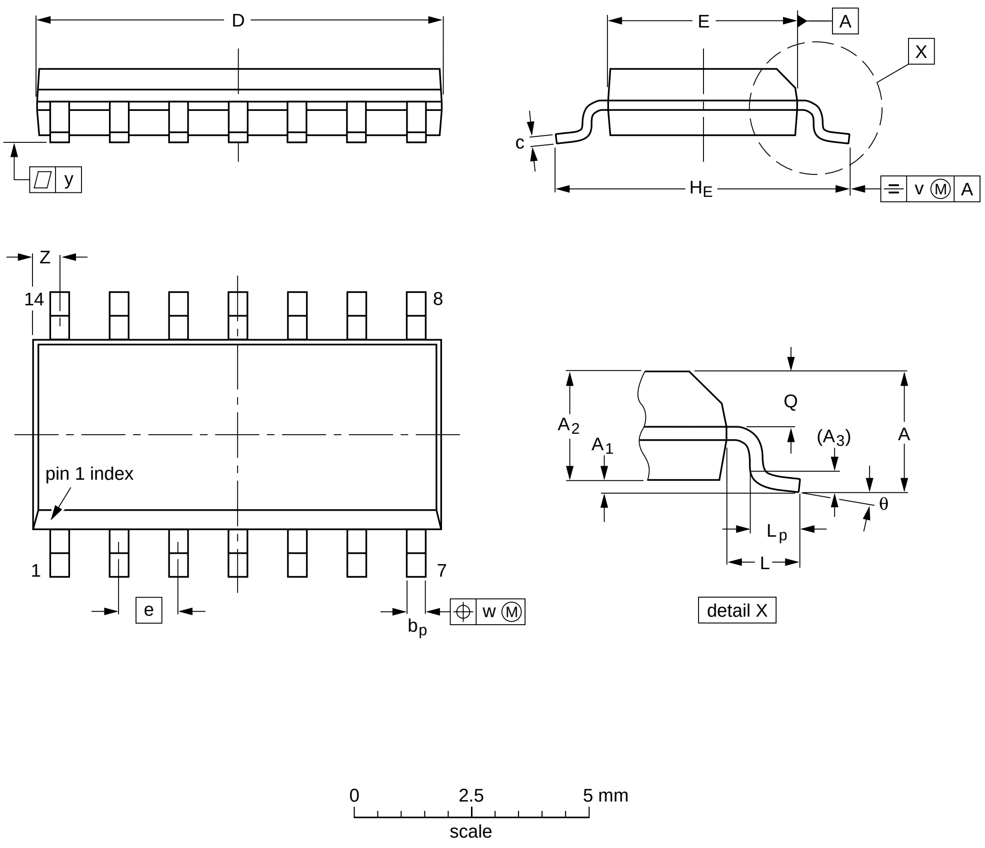
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 20. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

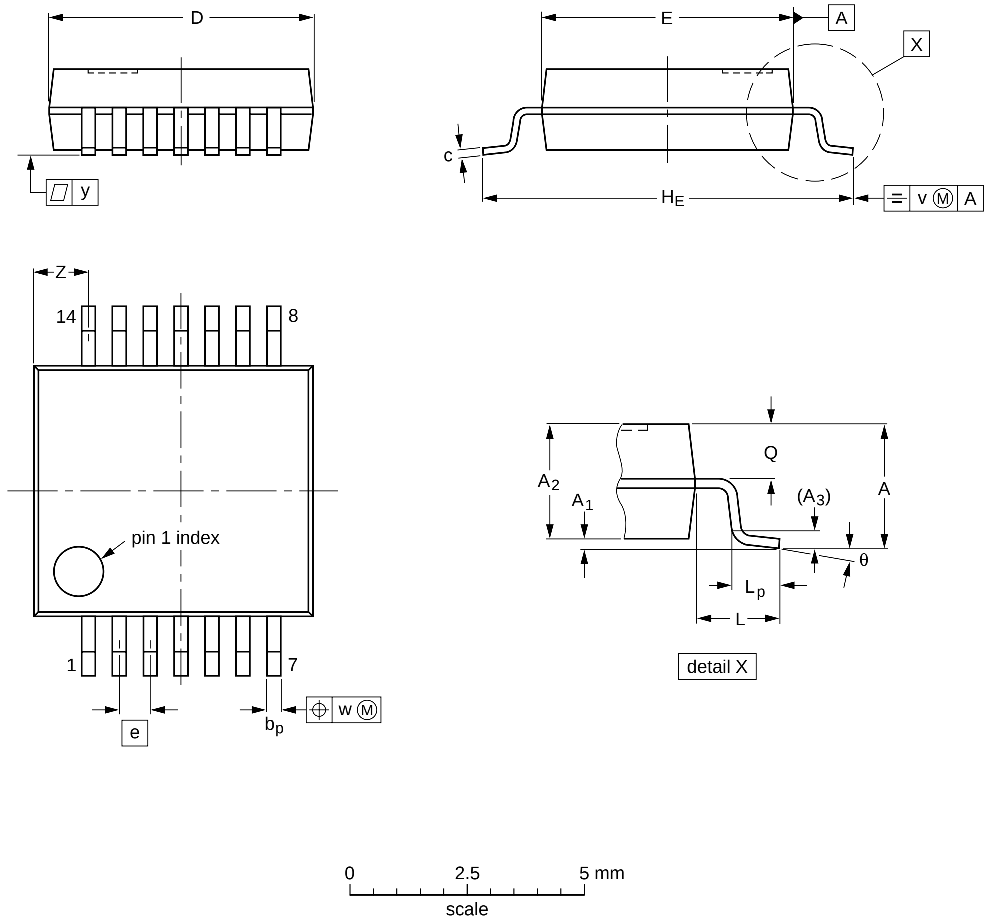
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 21. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

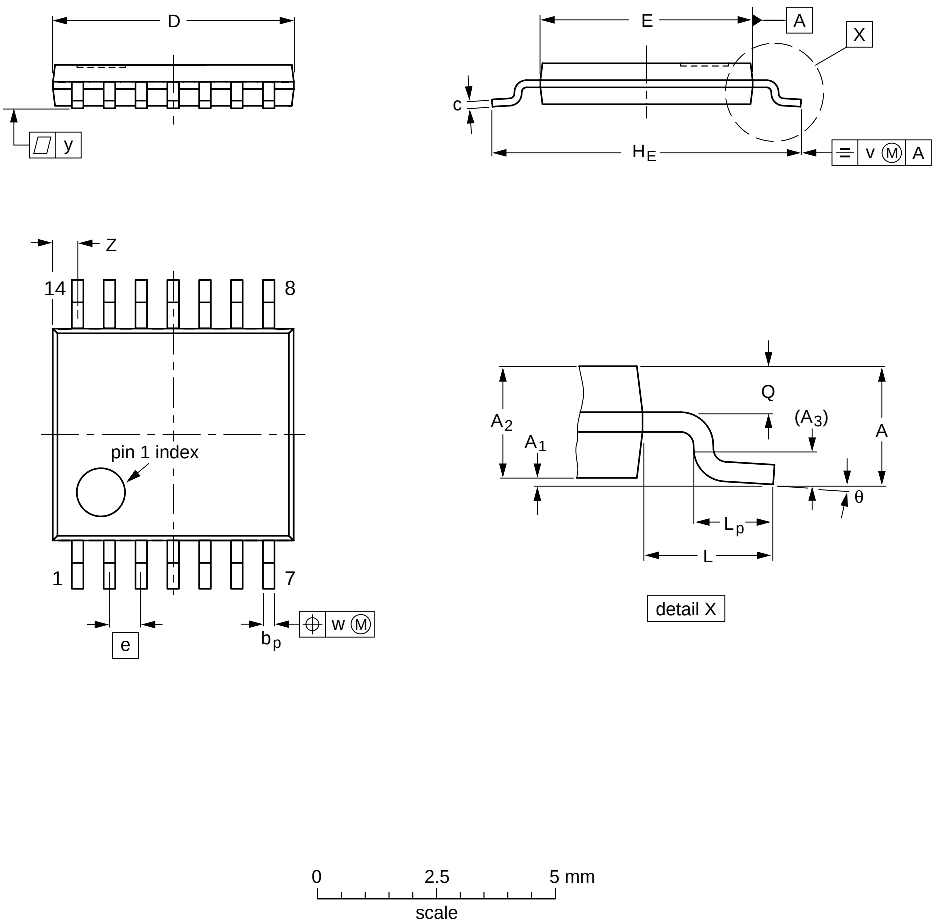
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 22. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 23. Package outline SOT402-1 (TSSOP14)

15. Revision history

Table 13: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LV4066_3	20050704	Product data sheet	-	9397 750 15209	74LV4066_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Table 2: corrected package names.				
74LV4066_2	19980623	Product specification	-	9397 750 04659	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

18. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

19. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

20. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

21. Contents

Date of release: 4 July 2005
Document number: 9397 750 15209

Published in The Netherlands